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(54) Recirculating loop memory array with a shift register buffer.

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Description

The present invention relates to a memory array including a plurality of recirculating memory elements, said memory elements being clocked in synchronism, so that the corresponding bits recirculate in their respective loops with the same time phase, and an input shift register having a number of cells equal in number to the number of said memory elements.

Such a memory array is known from IBM Technical Disclosure Bulletin Vol. 13 No. 7 December 1970, page 1879, which consists of a plurality of recirculating shift registers, which are connectable to a recirculating buffer shift register by a plurality of input/output gates. The data to be stored are entered into the buffer shift register serially and, controlled by a clock, are transferred in parallel, one bit of each word of the data to the memory shift registers. Due to the fact that a recirculating buffer shift register is used this memory array, which moves information into and out of the buffer shift register twice as fast as the movement of information within the memory shift registers, this known memory array can operate only in a staggered fashion and is principally not suitable for any other operation, particularly not for considerably higher speed.

Recirculating memories of the series-parallel-series type using charge coupled devices are known from ONDE ELECTRIQUE 1978 Vol. 58, No.4 pages 312 - 318, particularly figs. 6 and 9.

In order to really increase the operational speed of memory arrays having a plurality of recirculating loop memory elements that are buffered for parallel loading and fetching of data the invention proposes a memory of this type which is characterized by first input means for selectively connecting each cell to a respective one of said memory elements for simultaneously writing data into said memory elements in parallel, first output means for selectively connecting each cell to a respective one of said memory elements for simultaneously reading data from said memory elements in parallel, and by control means for clocking and shifting data into or out of said shift register through all the cells in the time interval between successive clocking steps of said memory elements.

Each recirculating element or loop is selectively connected to a respective shift register cell so that, on command, a particular recir culating bit in all of the loops can be fetched in parallel into their respective cells, and conversely, so that the bits stored in the shift register cells can be loaded in parallel into predetermined recirculating bits of their respective loops. By first loading all of the shift register cells with binary data, the corresponding bit in each of the recirculating loops can be loaded in parallel by selectively connecting the shift register cells to the recirculating loops. Then, the shift register is reloaded with new binary data and the next bit position in each of the recirculating loops is loaded in similar parallel fashion. This process is repeated until all of the bit positions in the recirculating loops have been loaded.

Data fetching is accomplished in an analogous manner. That is, a given corresponding bit position in each of the recirculating loops is loaded into a respective shift register cell and then the shift register is emptied of its stored data by shifting. Then the next bit in all of the recirculating loops is fetched into the respective cells of the shift register and the shift register is emptied as before.

The shift register is operated at logic speeds which are much faster than the bit recirculating rate of the memory loops. Consequently, the entire shift register is loaded in the interval between successive steppings of the bits in the recirculating loops, provided that the number of recirculating loops and, hence, the length of the shift register is not too extensive. In the case of extensive loop arrays, the array can be partitioned into groups of a smaller number of loops with a correspondingly shortened shift register selectively connected to each of the loop groups.

An embodiment of the invention is described below. The accompanying drawings show in

Fig. 1 a simplified block diagram of a CCD memory array adapted for data fetching and storing in accordance with the present invention; and in

Fig. 2 a simplified block diagram representing in greater detail a typical CCD loop of Fig. 1 and its selective connection to its respective shift register cell.

The memory array of Fig. 1 comprises a multiplicity of recirculating CCD loops 1, 2 ... N which preferably are individually addressible for writing and reading purposes associated with the storage of digital data. The loops are individually addressible by respective loop select signals on lines 3 at the outputs of address decode 4. Loop address signals are applied via lines 5 from a source (not shown) located off chip 6 containing the loops. The serial bit outputs from each of the loops 1 through N are selectively applied to a respective shift register cell 1', 2' ... N' comprising shift register 7. Shift register 7 receives digital data from line 8 for the serial loading of the register stages. The data stored at any given time within register 7 can be serially shifted out via line 9 and driver circuit 10 and made available on output line 11. Shift register 7 is employed for the parallel data fetching and for the parallel data loading associated with the han-

dling of data signals as well as test signals with the CCD loop memory array at different times.

Apparatus is also provided for the serial data fetching and the serial data loading of an individually addressed loop. Input data is applied via line 31 in the presence of write commands on lines 34 and 48 supplied by command control 13. Similarly, data stored within any addressed loop is fetched via lines 60, 61 and 62, AND gates 50, 51 and 52, OR gate 36 AND gate 37 (when conducting) and driver 38. Gate 37 is rendered conductive by a read command on line 39.

Command signals for the fetching and storing of data in the array loops are applied by lines 12 to command control timing logic 13. Phase clocks for the control of shift register 7 and the array loops are applied by lines 14 to command control and timing logic 13. The phase clocks are of such frequency and phase to permit the entire shift register 7 to be loaded or unloaded in the time between the stepping of data from one bit position to the next position within each of the recirculating loops. Stepping clocks are applied to loops 1 through N via line 40. Shift clocks are applied to the individual shift register stages via line 15. Parallel read and parallel write commands are applied by lines 16 and 17, respectively, to the individual shift register stages. Parallel read command signals and serial read command signals are applied alternatively to lines 16 and 39, respectively, by command control 13. The same alternative application is made of the parallel write command signals and serial write command signals to lines 17 and 48, respectively.

Referring now to Fig. 2, the typical CCD loop of Fig. 1 comprises AND circuit 18, OR circuit 19, series-parallel-series CCD registers 20, 21 and 22 and regenerative amplifier 23. When there is no write command on line 34 during the read-write enable interval, AND circuit 25 produces a zero output which is inverted (26) to render AND circuit 18 conductive to each of the recirculating data bits. The recirculating loop is broken, by the non conductance of gate 18, upon the appearance of a write command on line 34. A signal appears on line 34 whenever a serial write command occurs on line 48 or a parallel write command occurs on line 17. Input data gate 27 conducts in the simultaneous presence of a respective parallel write command signal on line 17 and input data on line 29. The output of gate 27 is coupled into the loop via OR circuit 19. Data is read out of the recirculating loop via AND gate 30 and line 32 upon application of a parallel read command on line 16 and in the absence of a write command signal on line 34.

Loop data signals are applied to AND gate 50 along with the respective loop selection signal on line 3. The output of gate 50 on line 49 is applied to OR gate 36. Write command signals are applied to AND gate 25 together with the respective loop selection signal on line 3. The serial input data bits are introduced into the loop via line 31 and OR circuit 19. The recirculating bits are blocked, during the writing interval by the non-conduction of gate 18 due to the conduction of gate 25 and the inversion provided by inverter 26, as previously explained.

It can be seen from the preceding specification that provision is made, in accordance with the present invention, for the parallel accessing of any addressed loop for data storage and fetching purposes as well as for the serial accessing of all loops at the same time. In the former instance, one corresponding bit is extracted from each of the loops and is applied to the respective stage of an output shift register. The register is shifted at a high rate so that its contents may be emptied (or filled, as the case may be) in the time interval between successive steppings of the recirculating loop bits. The parallel loop accessing mode is of special importance when utilized either as a high speed storage testing facility or as a cache data buffer. It also provides a paging hierarchy organization whereby data is distributed between all loops rather than within a single loop.

Claims

1. A memory array including a plurality of recirculating memory elements (1, 2 .. N), said memory elements being clocked in synchronism, so that the corresponding bits recirculate in their respective loops with the same time phase, and a shift register (7) having a number of cells (1', 2' ... N') equal in number to the number of said memory elements, characterized by first input means (17, 27, 29) for selectively connecting each cell to a respective one of said memory elements for simultaneously writing data into said memory elements in parallel, first output means (16, 30, 31) for selectively connecting each cell to a respective one of said memory elements for simultaneously reading data from said memory elements in parallel, and by control means (13, 15) for clocking and shifting data into or out of said shift register through all the cells in the time interval between successive clocking steps of said memory elements.

2. The memory array of claim 1 wherein the memory elements (1, 2 ... N) are charge coupled devices.

3. The memory array of claim 1, further including second input means (31, 47) independent of

the shift register (7) for writing data into the memory elements (1, 2 ...N).

4. The memory array of claim 1, further including second output means (50, 49, 36 - 38) independent of the shift register (7) for reading data from the memory elements (1, 2 ... N).

5. The memory array of claim 3 further including a command and control timing logic (13) for operating the first and second input means (17, 27, 29; 31, 47) and the first and second output means (16, 30; 50, 49, 36 - 38) alternatively.

Revendications

1. Réseau de mémoire comprenant une pluralité d'éléments de mémoire à recirculation (1,2...N), les dits éléments de mémoire étant impulsés en synchronisme, de sorte que les bits correspondants recirculent dans leurs boucles respectives avec la même phase de temps, et un registre à décalage (7) comportant un nombre de cellules (1',2'...N') égal au nombre de dits éléments de mémoire, caractérisé par des premiers moyens d'entrée (17,27,29) pour connecter sélectivement chaque cellule à un élément respectif desdits éléments de mémoire afin d'écrire simultanément des données dans lesdits éléments de mémoire en parallèle, des premiers moyens de sortie (16,30,31) pour connecter sélectivement chaque cellule à un élément respectif desdits éléments de mémoire afin d'extraire simultanément des données desdits éléments de mémoire en parallèle, et des moyens de commande (13,15) pour impulser et transférer des données à destination ou en provenance dudit registre à décalage à travers toutes les cellules dans l'intervalle de temps compris entre des impulsions successives desdits éléments de mémoire.

2. Réseau de mémoire suivant la revendication 1, dans lequel les éléments de mémoire (1,2,...N) sont des dispositifs à couplage de charge.

3. Réseau de mémoire suivant la revendication 1, comprenant en outre des deuxièmes moyens d'entrée (31, 47) indépendants du registre à décalage (7) pour écrire des données dans les éléments de mémoire (1,2...N).

4. Réseau de mémoire suivant la revendication 1, comprenant en outre des deuxièmes moyens de sortie (50, 49,36-38) indépendants du registre à décalage (7) pour extraire des données des éléments de mémoire (1,2,...N).

5. Réseau de mémoire suivant la revendication 3, comprenant en outre une logique de commande et de synchronisation(13) pour commander les premiers et les deuxièmes moyens d'entrée (17,27,29;31,47) et les premiers et deuxièmes moyens de sortie (16,30;50,49,36-38) alternativement.

Ansprüche

1. Speicheranordnung mit einer Anzahl von umlaufenden Speicherelementen (1, 2 ... N), die synchron gesteuert werden, so daß die entsprechenden Bits in ihren entsprechenden Speicherschleifen mit der gleichen Zeitphase umlaufen, und mit einem Schieberegister (7) mit einer Anzahl von Speicherzellen (1', 2' ... N') gleich der Anzahl der Speicherelemente, gekennzeichnet durch erste Eingabemittel (17, 27, 29) für eine selektive Verbindung jeder dieser Speicherzellen mit einem entsprechenden der Speicherelemente für ein simultanes paralleles Einspeichern von Daten in diese Speicherelemente, ferner durch erste Ausgabemittel (16, 30, 31) für eine selektive Verbindung jeder Speicherzelle mit einem entsprechenden der Speicherelemente für ein simultanes paralleles Auslesen von Daten aus den Speicherelementen, und durch Steuermittel (13, 15) für das taktmäßige Verschieben von Daten in das oder aus dem Schieberegister durch alle Speicherzellen hindurch in dem Zeitintervall zwischen aufeinanderfolgenden Taktimpulszeiten der Speicherelemente.

2. Speicheranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Speicherelemente (1, 2 ... N) aus ladungsgekoppelten Vorrichtungen bestehen.

3. Speicheranordnung nach Anspruch 1, dadurch gekennzeichnet, daß außerdem weitere von dem Schieberegister (7) unabhängige Eingabemittel (31, 47) zum Einschreiben von Daten in die Speicherelemente (1, 2 ... N) vorgesehen sind.

4. Speicheranordnung nach Anspruch 1, dadurch gekennzeichnet, daß ferner von dem Schieberegister (7) unabhängige Ausgabemittel (50, 49, 36 - 38) zum Auslesen von Daten aus den Speicherelementen (1, 2 ... N) vorgesehen sind.

5. Speicheranordnung nach Anspruch 3, gekennzeichnet durch eine Befehls- und Steuer- Taktgeberlogik (13), die der abwechselnden Betätigung der ersten und zweiten Eingabemittel

(17, 27, 29; 31, 47) und der ersten und zweiten Ausgabemittel (16, 30; 50, 49, 36 - 38) dient.

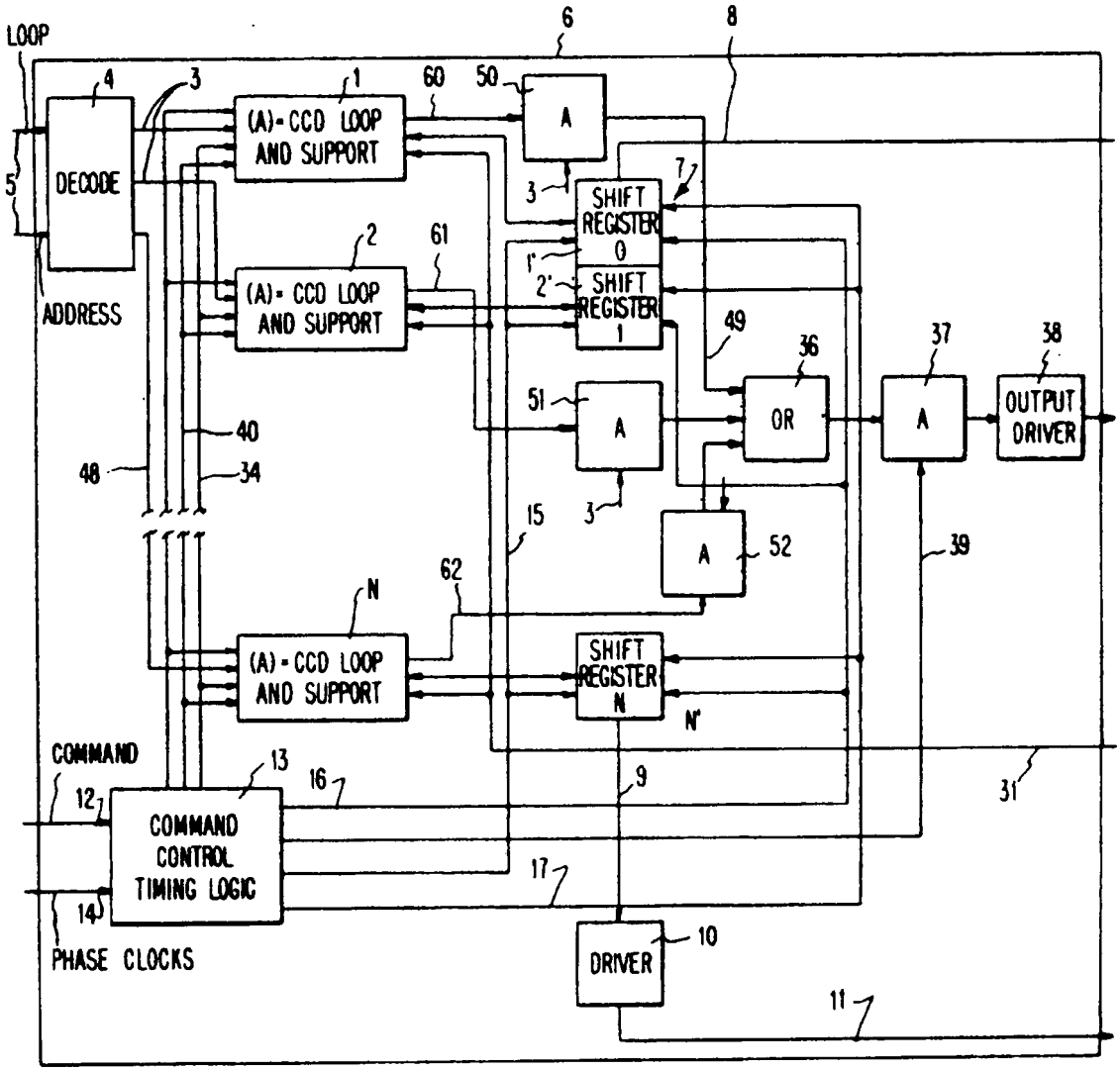
LOOP
6
8
4
3
1
60
50
A
DECODE
(A)-CCD LOOP AND SUPPORT
5
7
SHIFT REGISTER 0
2
61
1'
2'
SHIFT REGISTER 1
ADDRESS
49
36
37
38
51
A
OR
A
OUTPUT DRIVER
40
48
34
15
3
A
52
39
62
N
(A)-CCD LOOP AND SUPPORT
SHIFT REGISTER N
N'
COMMAND
13
12
16
9
31
COMMAND CONTROL TIMING LOGIC
17
14
PHASE CLOCKS
DRIVER
10
11

FIG. 1

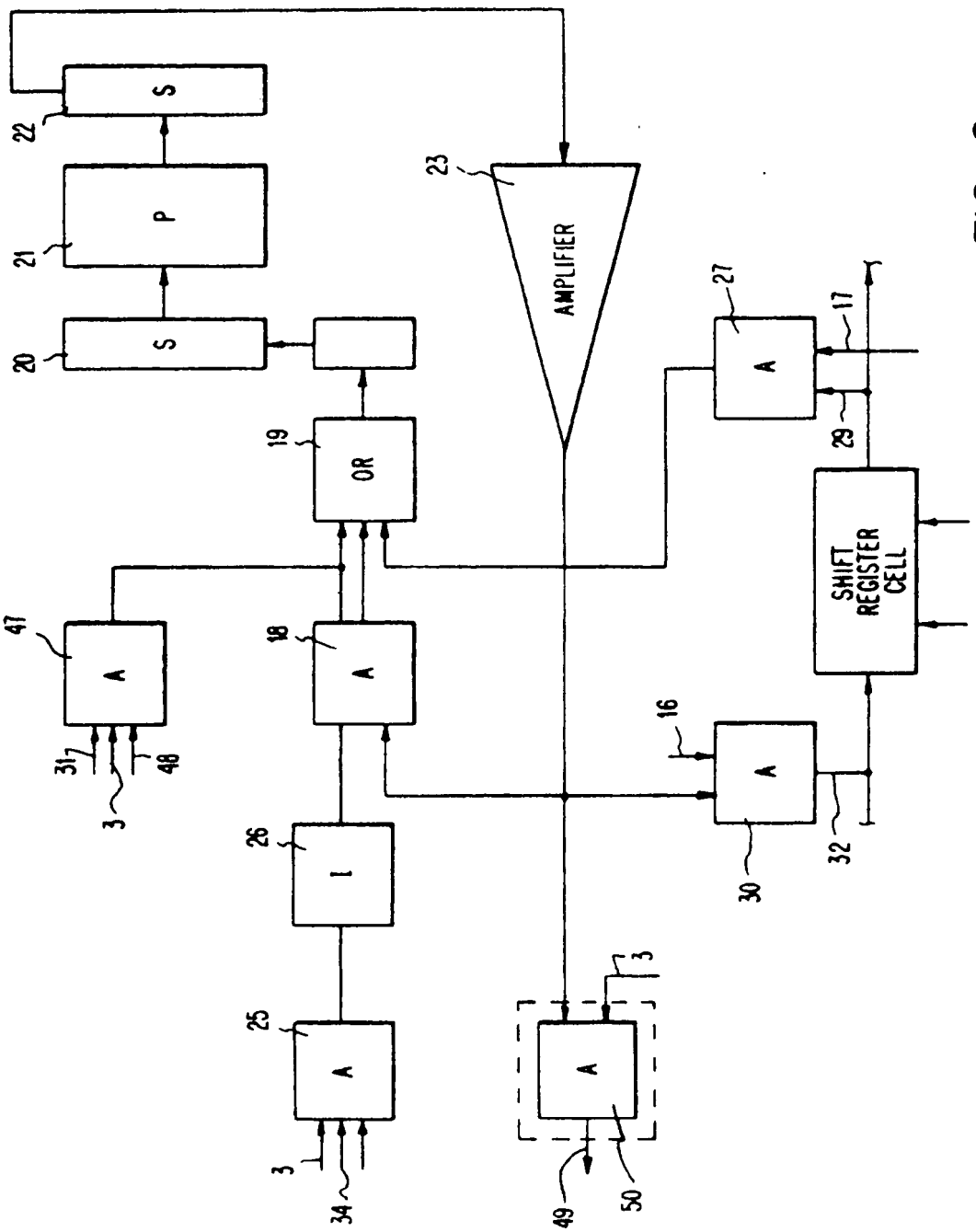
S
22
P
21
S
20
23
AMPLIFIER
19
OR
27
A
17
29
SHIFT REGISTER CELL
47
A
18
A
16
A
31
3
48
26
I
30
32
25
A
A
3
34
49
50

FIG. 2